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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :		(11) International Publication Number:
H01L 21/312, G03F 7/16	A1	WO 95/11521
		(43) International Publication Date: 27 April 1995 (27.04.95)

(21) International Application Number: PCT/GB94/02326

(22) International Filing Date: 21 October 1994 (21.10.94)

(30) Priority Data:
9321900.4 23 October 1993 (23.10.93) GB

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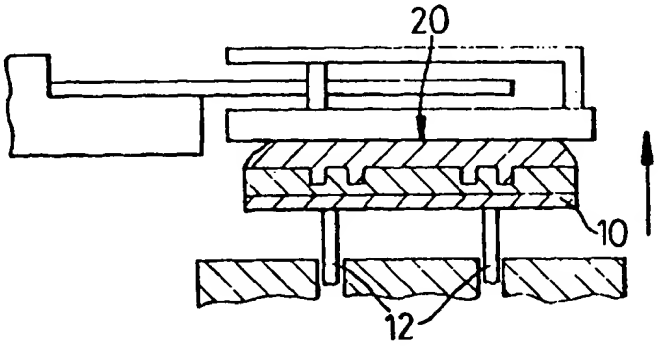
(81) Designated States: JP, KR, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: METHOD AND APPARATUS FOR THE PLANARIZATION OF LAYERS ON SEMICONDUCTOR SUBSTRATES

(57) Abstract

A semiconductor wafer (10) is provided with a planarization layer (14) which has its exposed surface (20) flatten by being engaged with a flat surface (19) on an anvil (16), which may be temporarily supported on the layer (14).



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METHOD AND APPARATUS FOR THE PLANARIZATION OF LAYERS ON SEMICONDUCTOR SUBSTRATES

This invention relates to method and apparatus for use in the treatment of semiconductor substrates and in particular, but not exclusively, when layers are deposited and etched on the substrate.

During the formation of semiconductor circuits on silicon wafers (and other semiconductors), a number of alternating layers of conducting and insulating films or layers is built up. The etching of the conducting layers to form interconnecting tracks causes an inherent "bumpiness" in the conducting layers. The application of a conformal dielectric layer to insulate one conducting layer from another enhances this surface "bumpiness". With reducing dimensions, the depth of focus of the lithographic equipment becomes incapable of accommodating the height variations caused by the lack of flatness in the built-up layers. Various techniques have been developed in an attempt to produce an insulating layer which gives a flat exposed surface ready for the next deposition. These include spin-on-glass; electron cyclotron resonance deposition; a planarisation treatment described in my International Patent Application No. PCT/GB93/01368 and chemical mechanical polishing. Only the last is capable of producing a surface which is flat within the terms accepted by the industry, typically optically flat, but it is a time consuming process.

In some of these techniques the insulating layer is at least for a time in a liquid state i.e. it is non-gaseous and capable of flowing at least at its exposed surface and at operational temperatures under moderate pressures.

From one aspect the invention consists in a method of forming a flat layer on semiconductor substrate, comprising forming a layer on the substrate in a liquid state and engaging the exposed surface of the layer, whilst the layer is still in the liquid state, with a flat or smoothing surface such that the exposed surface is flatten to conform with the flat or smoothing surface.

Preferably the flat surface and exposed surface are moved relative to one another to achieve engagement. In one embodiment, the flat surface may be formed on an anvil of sufficient mass to cause conforming flow in the layer. In this case the anvil may be suspended above the substrate and the substrate may be moved against the anvil to lift it from its suspended position.

Alternatively, the flat surface and the exposed surface may be pressed together by pneumatic pressure e.g. ambient or atmospheric pressure. In this case the flat surface may be formed on a plate or the like.

The flat surface and the exposed surface may be separated after flattening by gas or vapour being injected or formed between the surfaces.

Preferably the method is carried out in a vacuum chamber in which the substrate is being processed.

In another embodiment the smoothing surface may be

provided by a roller, which may be one of a pair of nip rollers.

From another aspect the invention consists in apparatus for flattening a deposited layer, in a liquid state, on a semiconductor substrate, comprising a body having a flat or smoothing surface and means for causing relative movement between the flat or smoothing surface and the layer for causing conforming engagement between the flat or smoothing surface and the exposed surface of the layer.

In one embodiment the apparatus includes an anvil defining the flat surface, means for suspending the anvil above the exposed surface and means for lifting the substrate so that it engages the exposed surface against the flat surface and lifts the anvil from its suspended position.

In another embodiment the smoothing surface may be provided by a roller, which may be one of a pair of nip rollers.

Although the invention has been defined above, it is to be understood that it includes any inventive combination of the features set out above or in the following description.

The invention may be performed in a number of ways, specific embodiments of which will now be described, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a schematic side view of apparatus for flattening a layer, in a liquid state, which has been deposited on a semiconductor substrate; the apparatus being

shown in its start position.

Figure 2 shows the apparatus of Figure 1, with an anvil above the layer;

Figure 3 shows the apparatus of Figure 1 with the layer and anvil engaged;

Figure 4 shows the apparatus of Figure 1 in the separated position after flattening, and indicates a separation device; and

Figure 5 illustrates schematically an alternative flattening apparatus.

In Figure 1 a semiconductor wafer 10 sits on a wafer support 11 which is provided with lifting pins 12. As can be seen, the wafer 10 has already been subjected to some treatment and there is thus an etched conducting layer 13 and a planarisation layer 14, which has been deposited on the conducting layer 13 and is still in a liquid state.

As usual the support 11 is contained within a vacuum chamber (not shown) and a wafer transfer mechanism 15 is provided for moving wafers into and out of the chamber. An anvil 16 is suspended on the spatula 17 of the wafer transfer mechanism 15 by means of a frame 18. The undersurface 19 of the anvil 16 is optically flat.

In Figure 2, the wafer transfer mechanism has been moved into the position in which it overlies the support 11 and hence holds the anvil 16 with its surface 19 immediately above the exposed surface 20 of the planarisation layer 14.

As can be seen in Figure 3, the pins 12 then lift the complete wafer 10 to engage the exposed surface 20 against

the flat surface 19. This engagement causes local conforming flow in the exposed surface 20, so that the hills and valleys 21,22 (see Figures 1 and 2) are smoothed out until the exposed surface 20 completely conforms with the flat surface 19.

If the planarisation layer 14 is formed as described in International Patent Application No. PCT/GB93/01368 water vapour will be given off and in the reduced pressure conditions this should be sufficient to provide for separation of the surfaces 19,20 when the pins are lowered (see Figure 4). However, if this does not occur, or if the system is used with some other planarisation layer, separation can be achieved or enhanced by introducing gas between the surfaces through line 23.

The above mechanism is particularly convenient because it enables the flattening to take place within the chamber in which planarisation deposition took place and so it prevents the planarisation layer going off before flattening occurs. However, in other circumstances, it may be perfectly proper to have a separate flattening chamber and in that case a fixed flattening surface may be provided. In a further variation a thin plate may be placed on top of the planarisation layer and the pressure in the vacuum chamber raised so that the flattening force is essentially pneumatic. Conveniently the chamber can be raised to atmospheric pressure.

Normally the planarisation will however take place at low temperatures and pressures and an appropriate anvil

temperature or its equivalent may be desirable or necessary.

An alternative approach is illustrated in Figure 5. Here the wafer 10, and its deposited layers 13 and 14, are passed between nip rollers 24 to flatten the layer 14. The process could be achieved in single or multiple passes or the rollers could be reversed several times so that the wafer 10 moves back and forth between them.

Claims

1. A method of forming a flat layer on a semiconductor substrate comprising, forming a layer on the substrate in a liquid state and engaging the exposed surface of layer, whilst the layer is still in the liquid state, against a flat or smoothing surface such that the exposed surface is flatten to conform with the flat or smoothing surface.

2. A method as claimed in Claim 1, wherein the flat surface and the exposed surface are moved relative to one another to achieve engagement.

3. A method as claimed in Claim 1 or Claim 2, wherein the flat surface is formed on an anvil of sufficient mass to cause conforming flow in the layer.

4. A method as claimed in any one of the preceding Claims, wherein the anvil is suspended above the substrate and the substrate is moved against the anvil to lift it from its suspended position.

5. A method as claimed in Claim 1 or Claim 2, wherein the flat surface and the exposed surface are pressed together by the ambient pressure.

6. A method as claimed in any one of the preceding Claims, wherein the flat surface and the exposed surface are separated after flattening by gas or vapour being injected or formed between the surfaces.

7. A method as claimed in any one of the preceding Claims, wherein the method is performed within a vacuum chamber.

8. A method as claimed in Claim 1, wherein the smoothing

surface is the surface of a roller.

9. A method as claimed in Claim 8, wherein the substrate and layer are past through a pair of nip rollers.

10. A method substantially as hereinbefore described, with reference to the accompanying drawings.

11. Apparatus for flattening a deposited layer, in a liquid state, on a semiconductor substrate comprising a body having a flat or smoothing surface and means for causing relative movement between the flat or smoothing surface and layer for causing conforming engagement between the flat or smoothing surface and the exposed surface of the layer.

12. Apparatus as claimed in Claim 11, including an anvil defining the flat surface, means for suspending the anvil above the exposed surface and means for lifting the substrate so that it engages the exposed surface against the flat surface and lifts the anvil from its suspended position.

13. Apparatus as claimed in Claim 11, wherein the suspending means include a semiconductor wafer transfer mechanism.

14. Apparatus as claimed in Claim 11, including a roller for providing the smoothing surface.

15. Apparatus as claimed in Claim 14, including a pair of nip rollers through which the substrate and layer may pass.

16. Apparatus for flattening a deposited layer on a semiconductor substrate substantially as hereinbefore defined.

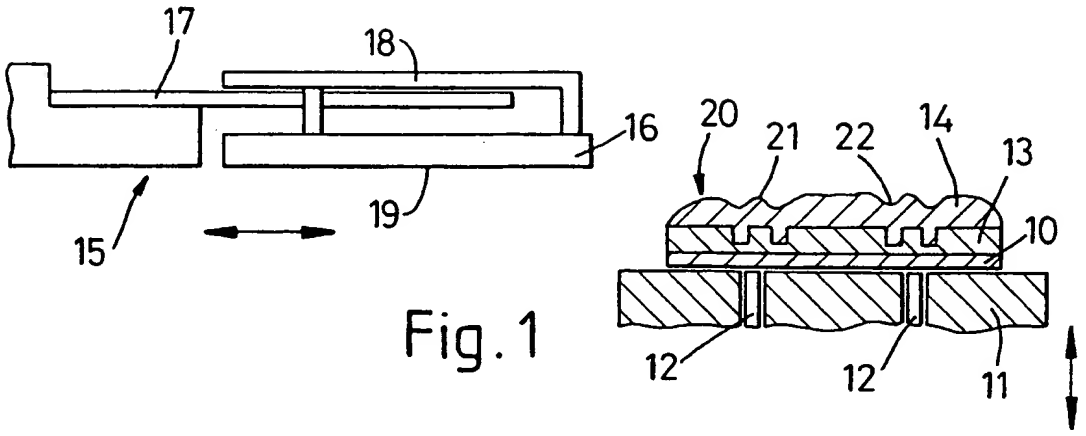

Fig. 1

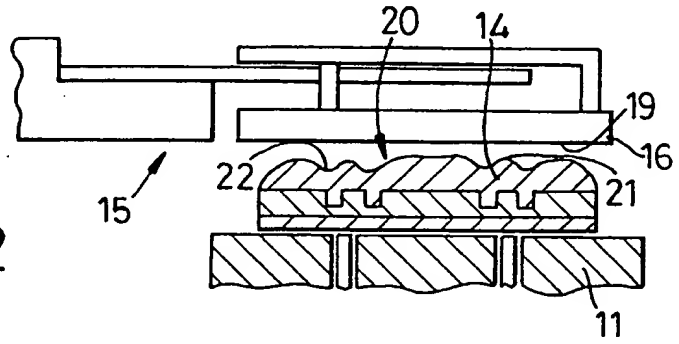

Fig. 2

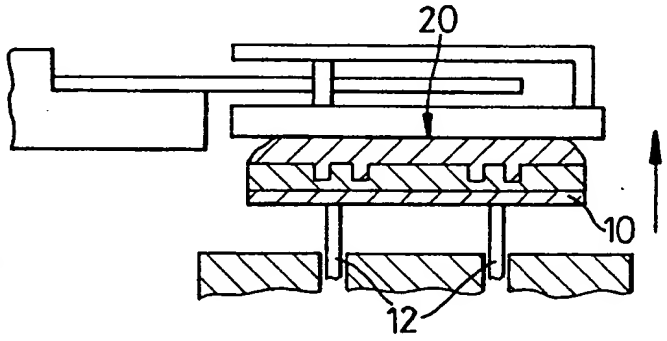

Fig. 3

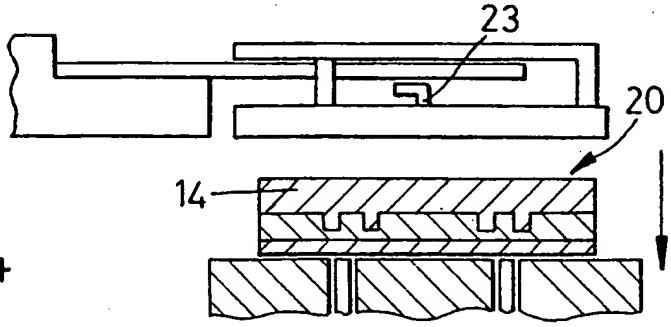

Fig. 4

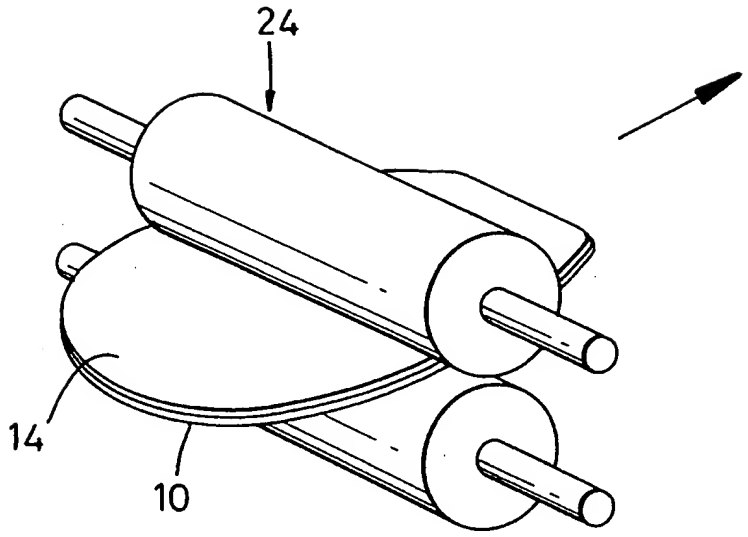

Fig. 5

INTERNATIONAL SEARCH REPORT

Interna l Application No
PCT/GB 94/02326

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/312 G03F7/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	IBM TECHNICAL DISCLOSURE BULLETIN., vol.27, no.1B, June 1984, NEW YORK US pages 591 - 592 ANONYMOUS 'Planarization layers' see the whole document	1,3,5
Y	---	8,9
X	PATENT ABSTRACTS OF JAPAN vol. 11, no. 227 (E-526) 23 July 1987 & JP,A,62 045 045 (SAGAWA SEIJI) 27 February 1987 see abstract	1,3
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[X] Further documents are listed in the continuation of box C.

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Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	IBM TECHNICAL DISCLOSURE BULLETIN., vol.32, no.5A, October 1989, NEW YORK US pages 402 - 403 ANONYMOUS 'Device for planarizing structures surfaces' see the whole document	1-4,11
A	IBM TECHNICAL DISCLOSURE BULLETIN., vol.33, no.11, April 1991, NEW YORK US pages 381 - 382 ANONYMOUS 'Dry film resist punch and diaphragm laminator' see figures	4,12
P,X	PATENT ABSTRACTS OF JAPAN vol. 18, no. 357 (C-1221) 6 July 1994 & JP,A,06 091 223 (TOSHIBA) 5 April 1994 see abstract	8
Y	PATENT ABSTRACTS OF JAPAN vol. 14, no. 359 (E-0959) 3 August 1990 & JP,A,02 125 436 (NAKANO) 14 May 1990 see abstract	8
Y	GB,A,2 018 314 (MIHURA ET AL) 17 October 1979 see abstract	9
A	IBM TECHNICAL DISCLOSURE BULLETIN., vol.32, no.1, June 1989, NEW YORK US pages 50 - 51 ANONYMOUS 'Leveling technique for pads of predeposited solder' see the whole document	9
P,X	PATENT ABSTRACTS OF JAPAN vol. 18, no. 176 (C-1183) 25 March 1994 & JP,A,05 337 438 (KATSUHIKO ET AL) 21 December 1993 see abstract	8

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INTERNATIONAL SEARCH REPORT

information on patent family members

Interr. al Application No
PCT/GB 94/02326

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB-A-2018314	17-10-79	JP-A- 54134407	18-10-79
		DE-A,C 2914585	18-10-79
		NL-A- 7902672	12-10-79
		US-A- 4298631	03-11-81